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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,099	01/31/2001	Yasuo Onishi	010093	1075

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NELSON, ALECIA DIANE.

ART UNIT	PAPER NUMBER
2675	[REDACTED]

DATE MAILED: 06/18/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

DA

Office Action Summary	Application No.	Applicant(s)
	09/774,099	ONISHI ET AL.
Examiner	Art Unit	
Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 31 January 2001.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-8 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3-5</u>	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), which papers have been made of record in the file.

Information Disclosure Statement

2. The references listed in the Information Disclosure Statement submitted on 06/12/96 have been made of record and has been considered by the examiner (see attached PTO-1449).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. **Claims 5-8** are rejected under 35 U.S.C. 102(e) as being anticipated by Kioke (EP 0953963).

The applied reference has a common inventor with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With reference to **claims 5-8**, Kioke teaches a pixel corresponding display device comprising a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal (see column 7, lines 45-50); an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit (see column 6, lines 40-43); calculation means for calculating, on the basis of a horizontal video start position closest to a horizontal period start position specified by the horizontal synchronizing signal out of horizontal video start positions detected within one field and a horizontal video end position detected within one field (see column 11, lines 29-41), the number of sampling clocks corresponding to the distance between the horizontal video start position and the

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horizontal video end position of the input video signal for the field; frequency adjustment means for controlling the clock generation circuit on the basis of the result of the calculation by the calculation means to adjust the frequency of the sampling clocks (see column 11, lines 50-57), judgment means for judging for each field whether or not the width of a region where input video exists is smaller than the number of horizontal effective pixels on the basis of the result of the calculation by the calculation means (see column 13, lines 54-column 14-12); and means for stopping, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels, a frequency adjustment operation based on the number of sampling clocks found in the field (see column 13, lines 19-31). With further reference to **claims 7 and 8**, Kioke also discloses a delay circuit, whose amount of delay is variable, for delaying and outputting a horizontal synchronizing signal of an input video signal (see column 11, line 58-column 12, line 4). With further reference to **claim 8**, Kioke discloses a detection circuit for comparing video data outputted from the analog-to-digital converter with a predetermined threshold value, to detect a horizontal video start position and a horizontal video end position on each of horizontal lines (see column 11, lines 17-41).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Koike (EP 00953963) in view of Haruhiko (JP 07264440).

With reference to **claims 1 and 3**, Koike discloses a display device comprising a clock generation circuit for generating sampling clocks, whose frequency is controlled on the basis of a required frequency control value, on the basis of a horizontal synchronizing signal of an input video signal (see column 7, lines 45-50); an analog-to-digital converter for sampling the input video signal on the basis of the sampling clocks generated from the clock generation circuit (see column 6, lines 40-43); horizontal video start position detection means for detecting a horizontal video start position of video data outputted from the analog-to-digital converter on the basis of a first threshold value, and a horizontal video end position detection means for detecting a horizontal video end position of the video data outputted from the analog-to-digital converter on

the basis of a second threshold value (see column 8, lines 23-37); calculation means for calculating the number of sampling clocks corresponding to the distance from the horizontal video start position to the horizontal video end position (see column 8, line 44-column 9, line 9); judgment means for judging whether or not the result of the calculation by the calculation means coincides with a required reverence value (see column 9, lines 9-19); frequency control value adjustment means for calculating, when it is judge that the result of the calculation by the calculation means and the reference value do not coincide with each other, a new frequency control value on the basis of the result of the calculation by the calculation means, the reference value, and the frequency control value currently set in the clock generation circuit, to feed the new frequency control value to the clock generation circuit (see column 9, line 51-column 10, line 1).

Koike fails to disclose a threshold value control means for controlling a second threshold value depending on the level of the video data outputted from the analog-to-digital converter, however does disclose problems that occur due to the set threshold values (see column 12, lines 39-44).

Haruhiko discloses a circuit, which automatically generates a threshold level in response to a received video signal and comparing the threshold level with the video signal (see abstract).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for such a circuit, as taught by Haruhiko, in a system similar to that which is taught by Kioke in order to thereby provide a method and

apparatus for controlling the threshold value based on the average level of the video data in order to avoid problems with noise in the video data.

With reference to **claims 2 and 4**, Koike teaches that the clock generation circuit further includes a voltage controlled oscillator (43), for outputting the sampling clocks, a frequency divider (44) for dividing the frequency of the sampling clocks outputted from the VCO (43), a phase detection means, to which an output of the frequency divider and the horizontal synchronizing signal of the input video signal are inputted, for outputting a detection signal corresponding to the phase difference between both the inputted signals, a filter means for integrating the detection signal outputted from the phase detection means to output the integrated detection signal to the VCO (43), and the frequency division ratio of the frequency divider being used as the frequency control value (see column 8, lines 6-37).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-9700.

adn/ADN
June 15, 2003



STEVEN SARAS
SUPERVISORY PATENT EXAMINER
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